Si/SiGe MMIC's

Johann-Friedrich Luy, *Member, IEEE,* Karl M. Strohm, Hans-Eckard Sasse, Andreas Schüppen, Josef Buechler, Michael Wollitzer, Andreas Gruhle, Friedrich Schäffler, Ulrich Guettich, and Andreas Klaaßen

***Abstract*—Silicon-based millimeter-wave integrated circuits (SIMMWIC's) can provide new solutions for near range sensor and communication applications in the frequency range above 50 GHz. This paper gives a survey on the state-of-the-art performance of this technology and on first applications. The key devices are IMPATT diodes for mm-wave power generation and detection in the self-oscillating mixer mode, p-i-n diodes for use in switches and phase shifters, and Schottky diodes in detector and mixer circuits. The silicon/silicon germanium heterobipolar transistor (SiGe HBT) with $f_{\max}$ values of more than 90 GHz is now used for low-noise oscillators at Ka-band frequencies. First system applications are discussed.**

I. Introduction

THE CHOICE of the substrate material is of essential importance for the planar integration of mm-wave circuits. The substrate has to fulfill a number of requirements: it has to be a mechanical carrier for the devices, as well as a low-loss dielectric for the waveguide structures. It has to be technologically suited for the fabrication of passive and active devices. These general requirements are met by silicon and GaAs. GaAs would be advantageous due to its semi-insulating properties, the higher electron mobility, and the direct bandgap transition which enables the realization of optoelectronic devices. The use of silicon as the base material for microwave integrated circuits has been discussed since 1965 [1]. This integration technique has been readdressed by an RCA group [2] and called "silicon millimeter wave integrated circuit" technology. Today, available silicon material with a resistivity of more than 10 kΩ·cm is suitable for planar circuits operated at frequencies above 40 GHz: the overall losses are dominated by the skin effect and radiation losses; the ohmic losses in the silicon substrate give only a minor loss contribution, typically on the order of 25% of the skin effect losses [3].

A number of mm-wave devices may now be realized in silicon: transit time diodes for power generation are operated in the saturated velocity regime, and IMPATT diodes are the most powerful millimeter-wave solid-state devices. Schottky diodes for operation in detectors and mixers are fabricated using conventional photolithography. p-i-n diodes for 76-GHz switches are realized by a two-step implantation. Recently, the silicon/germanium heterobipolar transistor appeared with current gain cutoff frequencies above 110 GHz and maximum oscillation frequencies above 70 GHz.

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J.-F. Luy, K. M. Strohm, H.-E. Sasse, A. Schüppen, J. Buechler, M. Wollitzer, A. Gruhle, and F. Schäffler are with Daimler-Benz AG, Research Center Ulm, D-89081 Ulm, Germany.

A. Klaassen and U. Guettich are with DASA, Ulm, Germany.

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II. Devices

The design of transit time diodes, p-i-n diodes, and some considerations on the design of HBT's are treated in this section. The layout of Schottky diodes is discussed in the technological section.

A. Transit Time Devices

Silicon IMPATT diodes are known to be powerful active devices. The possible output powers at 94 GHz of up to 1 W in CW operation [4], [5] are due to large modulation depths (up to 0.5), which lead to correspondingly low impedance levels. These impedance requirements can be met in waveguide technology. In planar integrated circuits, it is, however, difficult to achieve impedance values below 5 Ω. As the imaginary part of transit time diodes is usually a factor of 10–20 larger than the real part, the matching problem is mainly a question of real part matching. It is therefore essential to maximize the real part of the diode impedance via optimization of the doping profile and the geometry.

Flat profile double-drift IMPATT diodes already show an increase in the impedance level by a factor of 2 compared to single-drift devices. Fig. 1 shows lines of constant input power density in the impedance plane for the design frequencies 70 and 80 GHz where the drift region length is a parameter. The drift regions are assumed to be symmetrical. The impedance values are calculated from a large signal drift diffusion model. The optimum drift region length for 70 GHz operation is 300 nm, where the optimum is more pronounced at the lower input power density of 100 kW/cm^2. At this operation point, a real part of $-1 \cdot 10^{-5}\ \Omega \cdot \mathrm{cm}^2$ and an imaginary part of $-12.5\ \Omega \cdot 10^{-5}\mathrm{cm}^2$ is expected. Due to the large bandwidth negative resistance of IMPATT diodes, the drift region length optimum is almost unaffected by a shift to an operation frequency of 80 GHz.

A further increase of the impedance level is possible using the original Read diode approach [6]. From an analytical model, it can be seen that the internal conversion efficiency η_i of the diode follows:

$$\eta_i \propto \frac{l_d}{l_{dl}} = 1 - \frac{l_a}{l_{dl}}$$

with the depletion layer length l_{dl}, the drift region length l_d, and the avalanche region length l_a [5]. A confinement of the avalanche region length can be achieved by the introduction of doping spikes on both sides of the p–n junction in a double-drift diode. In a first-order design, the lower limit of the intrinsic avalanche region length in this double low–high–low

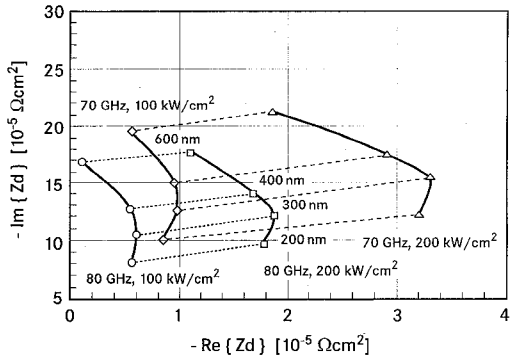

Fig. 1. Calculated lines of constant input power density in the impedance plane for two different frequencies (70 and 80 GHz) with the drift region length as a parameter. Double drift flat profile structure.

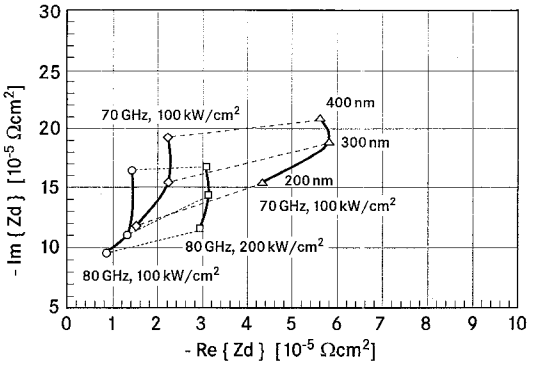

Fig. 3. Calculated lines of constant input power density in the impedance plane for two different frequencies (70 and 80 GHz) with the drift region length as a parameter. Double-drift low–high–low structure.

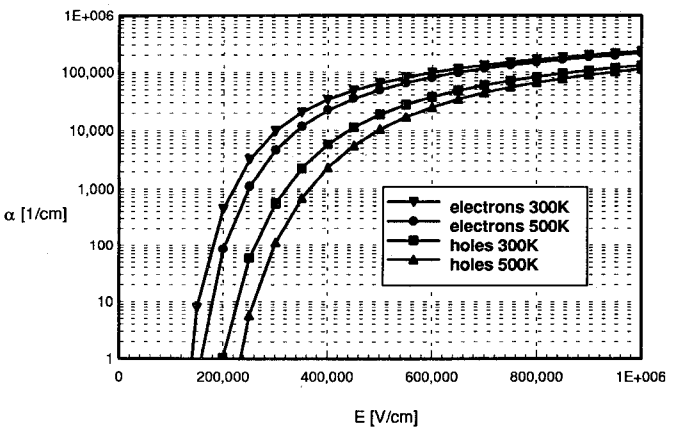

Fig. 2. Avalanche ionization rate of electrons and holes as a function of the electric field for two different temperatures.

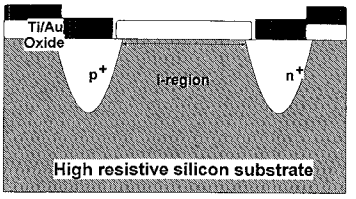

Fig. 4. Planar p-i-n diode concept.

(DLHL) diode is given by the breakdown condition

$$\alpha_{\text{eff}} 1_a \approx 0.85$$

where the effective ionization rate is given by [7]

$$\alpha_{\text{eff}} = \frac{\frac{\alpha_p}{\alpha_n} - 1}{\ln\left\{\frac{\alpha_p}{\alpha_n}\right\}} \alpha_n$$

with the ionization rate α_n for electrons and α_p for holes. The factor 0.85 is empirically determined and attributed to the fact that carriers drift already in the avalanche region.

Fig. 2 shows the ionization rates as a function of the electric field at two different temperatures as a fit to measurement results [8] using the Thornber expression [9]. At an electric field of $7 \cdot 10^5$ V/cm, an effective ionization rate of 65 000 cm^{-1} results, which leads to a minimum required avalanche region length of 130 nm. The sheet carrier density in the doping spikes is designed to guarantee a sufficient electric field in the drift region to reach the saturation velocity.

Fig. 3 shows the impedances of a DLHL diode in the impedance plane again on lines of constant input power density with the drift region length as a parameter for 70 and 80 GHz. We can see that the influence of the drift region length on the real part is even weaker as in flat profile structures. However, the absolute value of the real part is more than a factor of two larger in DLHL diodes: $2.2 \cdot 10^{-5}\ \Omega \cdot \text{cm}^2$ at 70 GHz with a drift region length of 300 nm at an input power density of 100 kW/cm^2!

B. p-i-n Diodes

The "on" resistance of p-i-n diodes may be described by

$$R_{\text{on}} = \frac{w_i^2}{(\mu_n + \mu_p) I_f \tau}$$

which shows the favorable influence of a large effective carrier lifetime τ in the I region. In bulk silicon, we expect mobilities $\mu_n = 1500\ \text{cm}^2/\text{V} \cdot \text{s}$ for electrons and $\mu_p = 450\ \text{cm}^2/\text{V} \cdot \text{s}$ for holes. With an effective carrier lifetime of $2 \cdot 10^{-4}$ s, the "on" resistance of silicon p-i-n diodes is far below 1 Ω at a forward current of 20 mA. If biased in the reverse direction, the I region is fully depleted and a constant capacitance of

$$C = \epsilon \frac{A}{W_i}$$

is obtained. We expect a capacitance of 62.5 fF for an effective i-region width of 0.4 μ m and an area $A = 5\ \mu\text{m} \cdot 50\ \mu\text{m}$.

The concept for the realization of a planar p-i-n diode without any epitaxial processes is illustrated in Fig. 4. The high resistive silicon substrate provides the i-region; the p^+ and n^+ contact layers are formed by implantation. The i-region width and the capacitance of the diode can be adjusted by changing the distance of the implantations.

C. High $f_{\max}$ HBT's

Recently, f_T values above 100 GHz have been reported for SiGe–HBT's [10], [11]. However, for most electronic

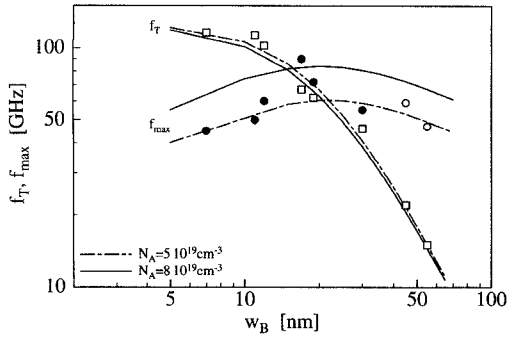

Fig. 5. Comparison of calculated and measured $f_{\max}(\bullet)$ and $f_T(\square)$ data. Open circles are estimated from f_T. Calculation (——): C: 150 nm/2·10^{17} cm^{-3}; B: 30% Ge; E: 70 nm/1·10^{18} cm^{-3} area 2·0.8·8 μm^2; V_{CE} = 3 V, $\mu_n \approx 200$ cm^2/V · s.

applications, the maximum oscillation frequency $f_{\max}$ is the figure of merit, e.g., low-noise amplifiers, oscillators [12], and mixers. In addition, high $f_{\max}$ values improve the noise behavior of HBT's with so far achieved 1.2 dB at 10 GHz [13]. The maximum oscillation frequency may be expressed as

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}.$$

This formula determines the important device parameter for attaining high $f_{\max}$ values in bipolar transistors, namely, a high cutoff frequency f_T and a low base resistance R_B and a low collector–base capacitance C_{BC}.

The advantage of SiGe–HBT's over standard bipolar transistors results from the possibility of doping inversion of the emitter and the base, i.e., the base can be higher doped than the emitter. Hence, low base sheet resistances are attainable also with thin bases down to 10 nm, e.g., a typical high-frequency bipolar transistor with base widths of less than 100 nm reaches base sheet resistances in the 10 k$\Omega/\square$ region, whereas SiGe–HBT's exhibit sheet resistances of approximately 1 k$\Omega/\square$ for a 20 nm doped base. The base width is the essential parameter for obtaining high f_T values. In reality, the tradeoff between low base resistance and high cutoff frequency limits the $f_{\max}$ values, as can be seen in Fig. 5 [14].

Analytical calculations predict the f_T values, and show that a maximum exists for $f_{\max}$ as a function of the base width w, in agreement with the measurements [15]. This is due to the increase of f_T with decreasing base width and the simultaneous rising base sheet resistance as discussed above. The measured S parameters were used without any deembedding to determine h_{21}, k, MSG, MAG, and the unilateral gain U. A device with 150-nm-thick and 2 · 10^{17} cm^{-3}-doped-collector, 15-nm nominal 30% SiGe base (8 · 10^{19} cm^{-3} boron), and 2- and 10-nm intrinsic spacers exhibits an $f_{\max}$ of 90 GHz at V_{CE} = 3 V with an emitter area of approximately 2·0.8·8 μm^2 [13]. This high $f_{\max}$ value results from a low base sheet resistance of only 0.4 k$\Omega/\square$ and a small C_{BC} of about 1–2 fF/μm^2 base area.

Further reduction of the transistor area and the collector–base capacitance by decreasing the collector doping concentration raises the maximum oscillation frequency to still higher frequencies [14].

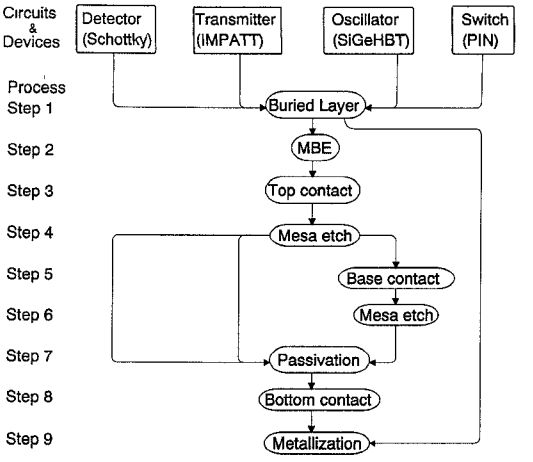

Fig. 6. Main steps of the SiGe/SIMMWIC technology.

III. Unified SiGe/SIMMWIC Technology

A simplified representation of the Si/SiGe SIMMWIC technology is shown in Fig. 6. For the fabrication of detectors, transmitters, oscillators, and switches, nearly identical technology steps are used. In all devices, buried layers are used. The further fabrication steps depend on the device type. For p-i-n diodes, only n^+ and p^+ buried layers are necessary; the intrinsic i zone is provided by the high-resistivity substrate. No epitaxial process is used. Therefore, only an additional metallization step is needed for the fabrication of p-i-n diodes.

For monolithic integrated Schottky barrier diode detectors, IMPATT diode oscillators, and SiGe HBT oscillators, the different active device layers are grown by silicon molecular beam epitaxy (Si–MBE). Usually, then, the top contacts are formed and mesa etches are performed. In the case of HBT devices, a base contact and a second mesa etch are needed. Next, the devices are passivated, the bottom contact is formed, and the final metallization layer is patterned. In the following, some basic fabrication steps and the fabrication of monolithic integrated p-i-n diodes, Schottky barrier diodes, IMPATT diodes, and SiGe HBT's are described.

A. Buried Layers

For the fabrication of monolithically integrated transmitter and receiver diodes and of bipolar and heterobipolar transistors in silicon substrates, highly conductive layers are needed. It is advantageous to form the highly conductive layers as buried layers. In this way, the devices can be manufactured in a quasi-planar configuration, and only mesa etches have to be performed. Depending on the device type, either highly conductive p^+ or n^+ buried layers are needed. The requirements for the buried layers are: low sheet resistance to minimize gap resistance and spreading resistance, high surface concentration to achieve a low contact resistance, and low defect density for the subsequent growth of defect-free epitaxial layers. There are several methods for forming highly doped diffusion layers: diffusion from a chemical source in vapor form at high temperatures, diffusion from a doped oxide source, and diffusion and annealing from an

ion-implanted layer. Annealing of ion-implanted layers is necessary for activating the implanted atoms and reducing the crystal damages resulting from ion implantation. When the annealing takes place at high temperatures, diffusion also occurs. Since ion implantation provides more precise control of total dopants from 11^{11} cm^{-2} to greater than 10^{16} cm^{-2}, it replaces the chemical or doped oxide source wherever possible. For n^+ buried layers, an As implantation process is used. This buried layer process is performed in the following way. First, the wafers are thermally oxidized to a thickness of 1.3 μm. By a photolithographic step, the oxide windows are defined and etched wet chemically. After a cleaning step, a 20-nm-thick scatter oxide is grown. This scatter oxide prohibits channeling effects during ion implantation. Then the As implantation is performed with a dose of $2 \cdot 10^{16}$ cm^{-2} and an energy of 100 keV. Annealing is performed at 1200° C for 5 h. This yields a sheet resistance of 4.3 $\Omega/\square$ and a surface concentration of $9 \cdot 10^{19}$ cm^{-3}. The homogeneity of the sheet resistance over a 4-in. wafer is better than 1%. The defect density is less than $2 \cdot 10^4$ cm^{-2} for all processes.

For the fabrication of monolithically integrated IMPATT diodes, it is advantageous to grow the active layers on an etch-stopping p^+ buried layer. For the formation of p^+ buried layers, a diffusion process is used which was originally developed for the fabrication process of silicon X-ray mask membranes [16]. The diffusion is performed at 1150°C for 50 min. with ramping. The wafers are positioned between BN sources. A sheet resistance of 2.5 $\Omega/\square$ is achieved; the junction depth is 4.1 μm. The boron concentration near the surface lies within a depth of 2 μm over 10^{20} cm^{-3}.

B. Silicon Molecular Beam Epitaxy (Si–MBE)

Most epitaxial processes use chemical-vapor deposition (CVD) techniques. A different approach is molecular beam epitaxy (MBE) which uses an evaporation method. Since CVD is a high-temperature deposition technique (850–1000°C) where the achievable doping profiles are limited by solid-state outdiffusion and autodoping effects, MBE is much more suitable for SIMMWIC technology. Si–MBE offers the following advantages: low growth temperature (450–750°C), precise control of thickness with submicron resolution, precise control of doping distribution, automatically abrupt interfaces and junctions, flexibility in the choice of material combination and layer structures, growth of heterostructures (Si/SiGe), and growth of superlattices.

MBE utilizes the clean environment of an ultrahigh vacuum (UHV) system for the growth of single crystalline films on oriented substrates. An industrial, single-slice, fully automatic, computer-controlled Si–MBE apparatus as described in [17] is used. By using Si–MBE, the active layers for basic SIMMWIC devices such as Schottky barrier diodes, planar-doped barrier (PDB) diodes, Si/SiGe tunneling diodes, avalanche transit time diodes, bipolar, and heterobipolar transistors are grown. One of the simplest layer sequences is applied to Schottky barrier diodes. Here, 70–150 nm thick epitaxial layers with doping concentration between $1 \cdot 10^{16}$–$2 \cdot 10^{17}$ cm^{-3} are grown on highly doped buried layers. Both p- and n-type Schottky barrier diodes can be grown. An example for IMPATT diode layer structures is given in Fig. 7, which shows the SIMS profile of a DLHL–IMPATT structure grown on an n^+ buried layer for monolithic integration.

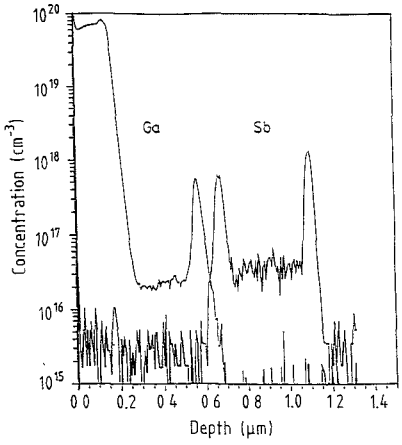

Fig. 7. SIMS profile of Si–MBE grown double low–high–low avalanche transit time diode.

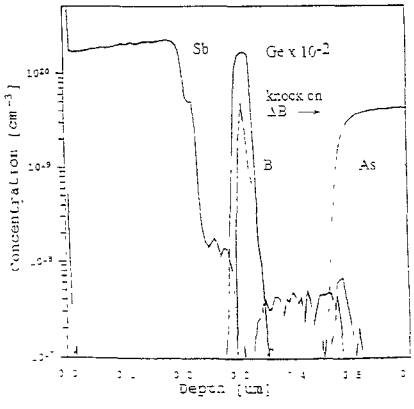

Fig. 8. SIMS profile of Si–MBE grown SiGe HBT structure.

Also, complete SiGe HBT layers are grown on 4-in. p^- substrates with As-implanted and subsequently diffused buried layers with 4.3 $\Omega/\square$ (Fig. 8). The wafers receive an RCA clean and an *in situ* 900°C flash-off. The 200-nm-thick collector is doped $3 \cdot 10^{17}$ cm^{-3} by Sb doping using secondary ion implantation. The SiGe base is grown at 530°C by coevaporation of Si and Ge, and starts with a 10-nm undoped spacer layer followed by a 20-nm, $2 \cdot 10^{19}$ cm^{-3} boron-doped layer. The boron flux is switched off shortly before the germanium in order to introduce a 1–2 nm thick emitter spacer layer. The $2 \cdot 10^{18}$ cm^{-3} Sb-doped emitter layer is 70 nm thick and grown by spontaneous dopant incorporation at relatively low temperatures between 425 and 450°C, followed by the 230-nm-thick n^+ emitter cap grown at 320°C to achieve 1–$2 \cdot 10^{20}$ cm^{-3} electrically active Sb concentration.

C. Fabrication Process of Planar p-i-n Diodes

For the fabrication of monolithically integrated lateral p-i-n diodes, the high-resistivity, undoped, or "intrinsic" silicon substrate itself is used for the intrinsic (I) zone. The $p^+(P)$

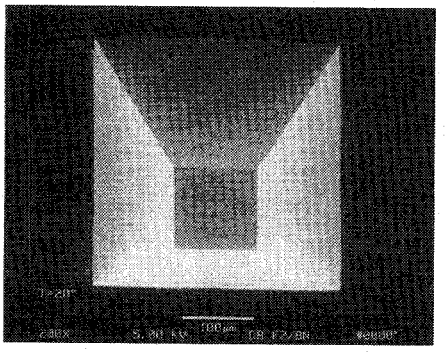

Fig. 9. Metallized via hole in a 100-μm-thick silicon substrate formed by anisotropic etching.

and $n^+(N)$ region are formed by standard buried layer processes. Selective ion implantation and simultaneous annealing are used. Therefore, the fabrication process of lateral p-i-n diodes is very simple. No epitaxy process is needed. The p^+ and n^+ contacts are also formed simultaneously with Ti–Au metallization.

Diodes with short i regions (1 μm) have been tested at Ka-band frequencies. Insertion loss of 1.5 dB and isolation of 30 dB were measured. Similar diodes are also integrated in a microstrip single-pole double-throw (SPDT) switch. In this case, via hole technology is used for grounding. The via holes are etched in a wet anisotropic silicon etch according to a method presented by Linde and Austin [18]. Via holes of pyramidal configuration are formed (Fig. 9).

D. Fabrication Process of Monolithic Integrated Coplanar Schottky Barrier Diodes

Schottky barrier diodes are efficient detector elements for millimeter waves. In order to use them in a receiver or mixer chip, they are realized in coplanar form. For proper working of these diodes in the millimeter wave region, the series resistance R_s and junction capacitance C_j should be as small as possible. To achieve the best mixer characteristics, the cutoff frequency $f_{co} = 1/2\pi R_s C_j$ is aimed to be ten times the detecting frequency. The junction capacitance is related to the diode area, doping of epitaxial layer, and diffusion voltage (barrier height). The series resistance is also related to the diode area and the doping of the epitaxial layer, but in an opposite sense. Therefore, an optimization of geometrical parameters (small area and minimal parasitic components) and doping parameters has to be performed to achieve a high cutoff frequency [19].

The fabrication process of the monolithically integrated planar Schottky barrier diodes is depicted in Fig. 10. High resistive silicon substrates with a resistivity $\rho > 4000\ \Omega \cdot$ cm are used. After forming an n^+ buried layer, a slightly doped n epitaxial layer is grown by silicon molecular beam epitaxy (Si–MBE). The doping concentration is $1{\cdot}10^{16}$ cm^{-3}; the layer thickness is 80 nm. Next, the Schottky anode contact is formed by photolithographic patterning and a lift-off process with 50-nm Ti, 50-nm Pt, and 300-nm Au. Then the epitaxial layer is plasma etched using the Schottky contact as etch mask. The ohmic contact is formed using a second life-off process with Ti, Pt, and Au metallization. The diodes are then passivated

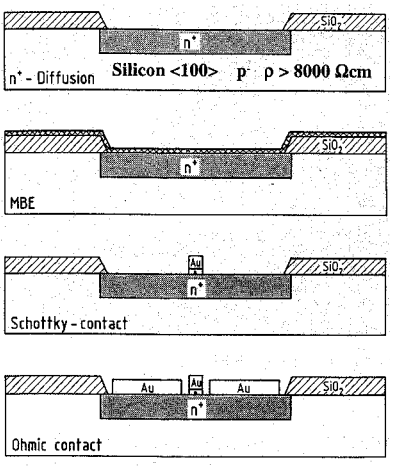

Fig. 10. Fabrication process of Schottky barrier diodes.

with a low-temperature PECVD silicon nitride. Finally, the gold pads are electroplated to a thickness of several μm.

DC measurements show an ideality factor of less than 1.08. The barrier height as determined from the saturation current is 0.5 V. CV measurements on mesa diodes yield a depletion width of 70 nm. This corresponds to a junction capacitance at zero bias of 1.5 fF/μm^2.

Diodes with a Schottky anode area of 12 μm^2 are mounted upside down in a single-ended mixer and tested at 94 GHz. With an LO power of 1 mW, a conversion loss of 10 dB is measured; with an LO power of 10 mW, a conversion loss of 6.5 dB is found. No bias is applied to the diodes (zero bias operation). These diodes are also integrated in slot line detectors.

E. Fabrication Process of Monolithically Integrated Transit Time Diodes

The fabrication process uses a self-stopping etchant, self-aligned contacts, silicon–nitride passivation, and air-bridge technology [20]. First, the high resistive ($\rho > 8000\ \Omega \cdot$ cm) silicon substrates are thermally oxidized and highly doped p^+ layers are formed by B diffusion. A sheet resistance smaller than 2.5 $\Omega/\square$ and a surface concentration greater than 10^{20} cm^{-3} are achieved. Next, the active layers of IMPATT profiles are grown by Si–MBE (see Fig. 4). The growth temperature is 550°C. Then the top contact of the IMPATT diode is defined, and the diode is mesa etched in a self-stopping etchant (aqueous KOH solution). A slight undercut is performed. This undercut enables self-aligned technology for defining the lower contact and reduces series resistance. To reduce surface leakage currents, the mesa edges are passivated by a 150-nm-thick, low-temperature (300°C), plasma-enhanced deposited Si_3N_4 film. Finally, air-bridge technology is applied for forming the top contact of the diode.

F. Heterobipolar Transistors for SIMMWIC's

Compared with the bipolar junction transistor, the SiGe HBT offers the possibility of a high base doping for a low base resistance, an accelerating field by grading the Ge content, a short base transit time by reducing the base thickness,

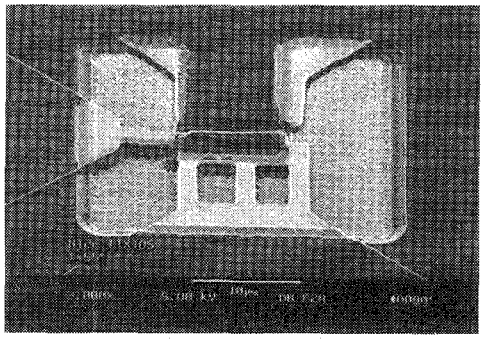

Fig. 11. SEM of an integrated HBT.

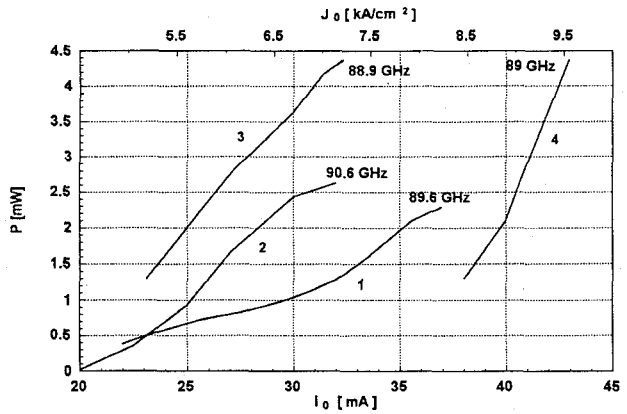

Fig. 12. Radiated CW power versus dc current, radiation through the substrate, substrate thickness: 100 μm, slot length: 1.6 mm^{+}. 1–3: Double low–high–low (DLHL) IMPATT structure, $\varnothing = 24$ μm; 4: quasi-Read double drift (QRDD) IMPATT structure, $\varnothing = 24$ μm.

and the elimination of the emitter delay. The growth of the complete transistor structure by MBE meets the demand of precise control of thickness, doping, and Ge content and avoids high-temperature processes.

For the fabrication of the device [13], a PtAu emitter metal is defined by lift-off, and acts as a mask for the following selective wet chemical etch which stops at the SiGe layer. The base metallization is self-aligned with respect to the emitter because of the controlled overetch. A dry etch gives access to the buried layer. After the collector metallization, a second dry etch forms deep trenches that separate the contact pads from the active area, leaving air bridges. Fig. 11 depicts the layout and scanning electron micrographs of air bridges and emitter undercut. The excellent FM-noise behavior makes them attractive for future monolithically integrated millimeter wave oscillators.

IV. Circuits

A. Transmitter

The monolithic transmitter circuit consists of a coplanar slot resonator also serving as the antenna where an IMPATT diode is monolithically integrated in the center of the slot [21]. Due to the high permittivity of silicon, more radiation is emitted through the substrate than directly into the air. Fig. 12 shows the CW power radiated from the backside of the chip into a W-band waveguide measurement system. No additional heat sink is applied. The maximum radiated power is 4.4 mW at 89 GHz with an S/N of -82 dBc at 100 kHz off carrier. It can be seen that the DLHL structures due to their higher impedance level have lower oscillation threshold currents than the QRDD (single-spike) devices. This operation mode is also extracted mounting the chip upside down on a metal carrier with an integrated cavity [22].

Furthermore, the slot transmitters are operated upside up with a grounded substrate. The maximum power radiated directly into the air is 1.3 mW at 75 GHz.

B. SPDT Switch

The layout of a monolithic single pole–double throw (SPDT) switch is shown in Fig. 13. The chip size of the SPDT is $3.3 \cdot 1.7$ mm^2. For operation at E-band frequencies, p-i-n diodes with 5-μm i-region width are used.

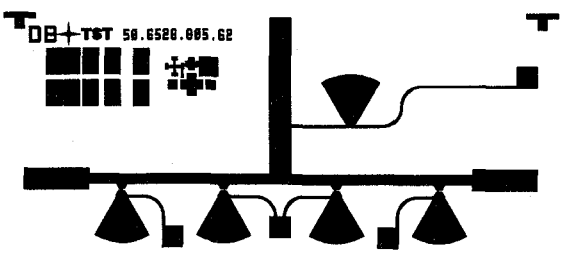

Fig. 13. Layout of the SPDT switch.

The SPDT comprises two symmetrical cells for the ON and OFF arm connected to a common input port. Each arm consists of two diodes in a parallel or shunt configuration, with one side connected to the ground. As RF-short, a radial stub is used, and the dc-short is achieved by a via hole and a small transmission line, $\lambda/4$ long. The via hole is transformed to an RF-open at the input port of the radial stub. In one arm, the anodes, and in the other arm, the cathodes of the two shunt diodes are connected to ground. With this antiparallel combination of the diodes in the different arms, only one bias supply $+/-Ud$ is necessary for biasing both arms. The bias is injected at the input line.

Millimeter wave measurements of the SPDT p-i-n switch were made in the E band from 60–90 GHz with a specially developed four-port waveguide test fixture. Broad-band transition from waveguide to microstrip is achieved with E probes. The test fixture is calibrated with 50-Ω microstrip transmission lines. The insertion loss for the ON state and the isolation in the OFF state of the SPDT switch are shown in Fig. 14. In the ON arm, the diodes are biased in the reverse direction by $Ud = -1.2$ V and simultaneously in the OFF arm in the forward direction with $Id = 20$ mA. In this frequency range of 67–80 GHz, the SPDT shows an insertion loss of 2.0–2.5 dB in the ON state. In the OFF state, the isolation was measured to be better than 25 dB.

C. HBT Oscillators

The topology for the 24-GHz DRO design for hybrid or monolithic application on high-resistivity Si substrate is a

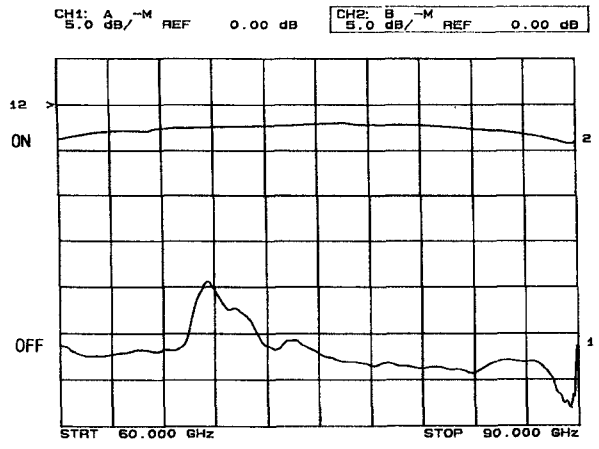

Fig. 14. Insertion loss and isolation of the p-i-n switch versus frequency.

state-of-the-art series feedback configuration using the HBT device in common emitter operation [23]. The dielectric resonator is placed at the base side of the transistor; the output port is at the collector side. The microstrip circuit is designed using small-signal S parameters of the HBT measured up to 40 GHz by means of an hp8510 network analyzer and in-house developed linear CAD software to characterize critical microstrip discontinuities such as T junctions or radial stubs. The dielectric resonator coupled to the microstrip is modeled as a lossy parallel resonant circuit. By optimizing the distance between resonator coupling locus and transistor base and the length of the emitter feedback line, the magnitude of the reflection coefficient at the output port (collector) is maximized. The output port, as seen in Fig. 15, is designed to match the collector impedance to a 50-Ω load with respect to the small-signal oscillation condition. The hybrid oscillator is fabricated on a 150-μm substrate (chip size $6 \cdot 6$ mm). HBT chips ($0.3 \cdot 0.5$ mm) are inserted into a hole made in the substrate and connected by gold leads to the microstrip lines. The 50-Ω termination at the transistor base applied to quench spurious oscillations is realized by a chip resistor adhered to the substrate. Bias networks consist of quarter-wavelength 75-Ω lines and 60° radial stubs. As dielectric resonators, barium–titanade pucks with a constant of 36 are used (diameter 2.7 mm, height 1.2 mm). In Fig. 16, the output spectrum of the DRO is shown. At 23.2 GHz, an RF power of +7 dBm with a phase noise of −92 dBc/Hz (100 kHz off carrier) is measured with an unpassivated HBT device.

V. Applications

A. Velocity Sensor

For various controlling tasks in a vehicle or a train, the velocity over ground has to be known. Conventionally, the velocity is measured via the number of revolutions of a wheel, for example. This may lead to an incorrectness of up to several percent due to slip. To resolve this problem, a millimeter wave radar sensor may be used. One method for sensing the velocity is to measure the Doppler frequency shift f_D:

$$f_D = \frac{2f_s}{c_0} v \cos\vartheta, \quad v\text{: velocity},$$

f_s: signal frequency, c_0: speed of light.

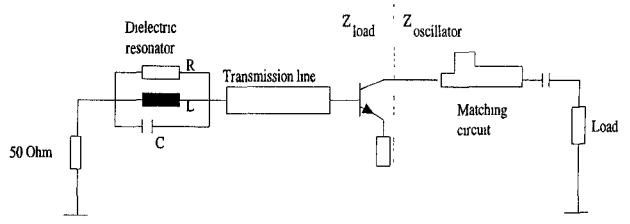

Fig. 15. Equivalent circuit of the HBT oscillator.

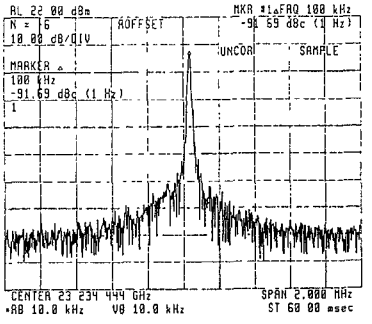

Fig. 16. Spectrum of the 23.2-GHz HBT oscillator on silicon substrate.

Basically, the sensor consists of three components: the millimeter wave chip, the antenna system, and the signal analysis. The millimeter wave chip is an integrated W-band IMPATT oscillator/transmitter which works as a self-oscillating mixer. This concept has advantages compared to the use of an external mixer, as it requires no additional (Schottky) diode, no LO, and no waveguiding structure. The MDS (minimal detectable signal) of a self-mixing IMPATT oscillator can be as low as −145 dBm at an offset of 10 kHz from the carrier at an oscillator power of −10 dBm [24].

The millimeter wave chip is placed on an electronic board which contains the dc current source for the IMPATT diode and an amplifier for the Doppler signal. The antenna system is formed by the radiating chip, the part of the housing which acts as a horn, and by a dielectric lens. The half-power beamwidth of the antenna pattern is 8.5°. This sensor is able to detect a Doppler signal at target velocities down to 0.1 m/s. The accuracy is better than 1%.

B. Moving Distance Sensor

In near-range systems, the time delay of a reflected signal is very small (6.67 ns/m). Thus, for sensing the distance of a target, it is more convenient to measure the phase difference of the transmitted and the received signal than the time delay. The small region of unambiguous range using a single-frequency signal may be extended considerably by the two-frequency CW radar using self-mixing oscillators [25]. The block diagram of the 2FCW radar employing the self-mixing oscillator concept is shown in Fig. 17.

For $f_{s1} > f_{s2}$, $dR(t)/dt < 0$ ($R(t)$ is the time-dependent object distance), the output spectrum of the two channels looks as depicted in Fig. 18. Both Doppler signals are present in the base band as well as in the IF band of both channels because of the coupling of the two transmitters. The information about the direction of motion of the target is in the IF band signals.

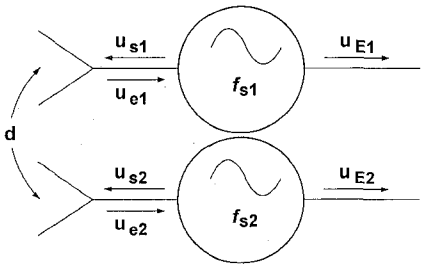

Fig. 17. Block diagram of a two-frequency CW radar with self-mixing oscillators.

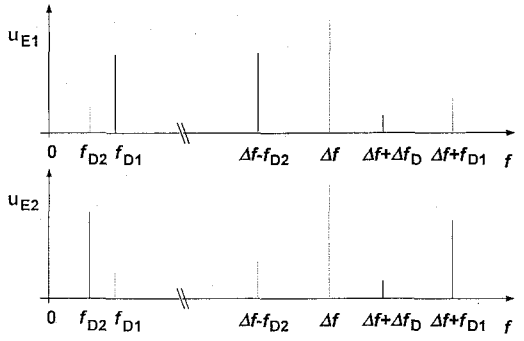

Fig. 18. Spectrum of channels 1 and 2 (without intermodulation products); dashed lines are present when the transmitters are coupled.

To analyze the phase difference of the two Doppler signals, the frequency shifts have to be approximately equal to one another ($f_{D1} \cong f_{D2}$), which means $\Delta f \ll f_{s1}$. Then the Doppler signals cannot be separated in the baseband, but in the IF band after mixing to lower frequencies. Thus, for a straightforward system, care has to be taken to avoid the coupling. In this case, the Doppler signals are given by

$$u_{D1} \propto U_{D1} \cos\left[\pm\omega_{D1} t - \frac{2\omega_{s1} r}{c}\right] \quad \text{and}$$

$$u_{D2} \propto U_{D2} \cos\left[\pm\omega_{D2} t - \frac{2\omega_{s2} r}{c}\right].$$

The phase difference is proportional to the distance of the target: $\Delta_{\varphi D} = 2\Delta\omega R_o/c$ and the unambiguous range is $R_{o,\max} = c/2\Delta f = \lambda_{\Delta f}/2$.

In the front end, four transmitter chips are arranged on a copper block. One chip of each pair works as the transmitter, and the other as a tuning circuit for stabilizing the difference frequency Δf. Additional steps formed by metal plates are used to suppress the coupling of the transmitters. The block is mounted at the feed of a horn antenna which is phase corrected by a dielectric lens.

The sensor is tested by measuring the phase difference of the Doppler signals in the baseband while varying the distance of a metal plate. The result is shown in Fig. 19. The main reason for the rather high variation around the theoretical curve is that the horn and the metal plate form a quasi-optical resonator. Hence, the oscillation frequencies of the transmitters are tuned by the external resonator. This phenomenon may be suppressed by locking the oscillators to a reference signal by subharmonic injection locking [26]. This can be achieved by the use of SiGe HBT oscillators operating at 1/3 of the mm-wave frequency to be stabilized.

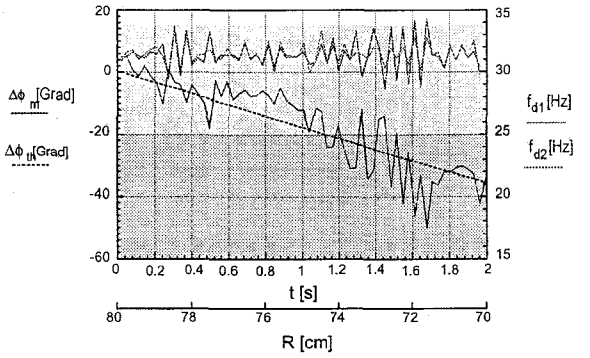

Fig. 19. Theoretical ($\Delta\Phi_{th}$) and measured ($\Delta\Phi_m$) phase difference and Doppler signals versus distance.

VI. Conclusion

First, Si/SiGe MMIC's and applications are demonstrated. One example is a Doppler sensor for near-range measurements. This sensor uses only one chip with a transit time diode in the self-oscillating mixer mode. The great advantage of the realized p-i-n switch compared to other technologies is the avoidance of epitaxial techniques. This means that this device type may be realized before other device layers are grown by epitaxy on the same wafer. Schottky diodes show a low conversion loss (6.5 dB) in 94 GHz mixers. Zero bias operation is possible due to the comparatively small energy gap of silicon. The frequency stability of two-terminal mm-wave sources is critical, especially in a planar technology. A solution to this problem is possible by the use of SiGe HBT VCO's or DRO's for subharmonic injection locking. One of the most promising aspects of this Si/SiGe MMIC technology is its potential compatibility with LSI techniques, e.g., CMOS circuits. This is, however, still the subject of future work.

Acknowledgment

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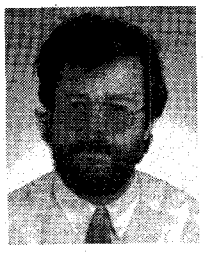
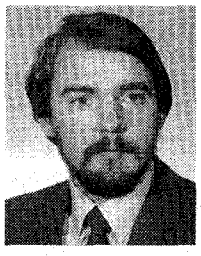


Johann-Friedrich Luy (M'86) was born in Stuttgart, Germany, in 1958. He received the Dipl-Ing. degree in 1983 for his investigations on heat conduction in semiconductor lasers. In 1988 he received the Dr.-Ing. degree for his thesis on the first silicon MBE-made IMPATT diodes from the Technische Universität München.

In 1983 he joined the Daimler-Benz Research Center (formerly AEG), Ulm, and worked on silicon IMPATT diodes. Since 1989 he has been engaged in research on Si/SiGe millimeter wave devices and circuits (SIMMWIC's), and has been responsible for this team since 1993. He served as a co-editor of the book, *Silicon Based Mm-Wave Devices*, which appeared in 1994.



Karl M. Strohm received the Diplom and Dr. rer. nat. degrees in physics, both from the University of Stuttgart, Germany, in 1974 and 1978, respectively, for his investigations on color centers in insulating crystals.

He served as a research assistant at the University of Stuttgart until 1980. Then, he joined the AEG Research Center, Ulm, Germany. There, he was first involved with yield statistics in the fabrication process of semiconductor devices and later with X-ray lithography. In 1989 he moved to Daimler Benz Research Center, Ulm, Germany, where he is now engaged in SIMMWIC (silicon monolithic millimeter waveintegrated circuit) technology.

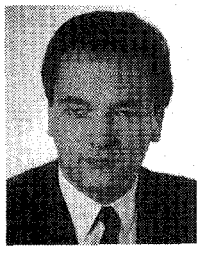
Hans-Eckard Sasse was born in Hardegsen, Germany, on April 28, 1946. He received the diploma and Ph.D degree in chemistry from the University of Heidelberg in 1970 and 1972, respectively.

He joined the Research Center of AEG-Telefunken in 1974 and has since worked on radioactive tracer studies, surface analytics (X-ray electron spectroscopy) and integrated millimeter-wave circuits, especially p-i-n switches.

Andreas Schüppen was born in Geilenkirchen, Germany, in 1961. He received the Dipl.-Ing. degree and the Ph.D. degree (Dr.-Ing.) from the RWTH Aachen in 1988 and 1993, respectively.

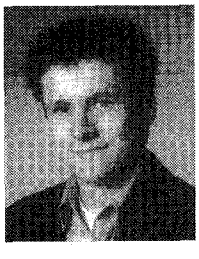
In 1988, he joined the Institute of Thin Film and Ion Technology at the Research Center, Jülich, Germany, where he worked on silicon permeable base transistors. He is now with the Daimler-Benz AG Research Center, Ulm, Germany, where he is examining SiGe–HBT's.

Dr. Schüppen was the recipient of the European Material Research Society Young Scientist Award in 1993.



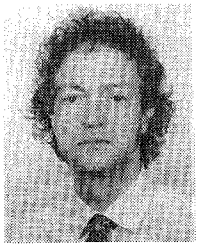
Josef Buechler was born in Pfaffenhofen, Germany, in 1956. He received the Dipl.-Ing. degree in electrical engineering in 1989, both from the Technical University of Munich, Germany.

From 1984 to 1989 he worked as a research assistant at the Technical University of Munich, where he was engaged in the design and development of silicon-based monolithic integrated millimeter wave circuits. In 1989 he joined the Daimler-Benz Research Center, Ulm, Germany, where he is currently engaged in the design and development of integrated mm-wave components and mm-wave sensor systems.



Michael Wollitzer was born in Landsberg, Germany, in 1967. He received the Dipl.-Ing. degree from the Technical University of Munich, Germany, in 1993.

Since then, he has worked as a research assistant at Daimler Benz Research, Ulm, where he is engaged in the development of solid-state oscillators and planar millimeter-wave circuits.



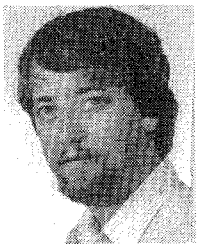
Andreas Gruhle was born in Heidelberg, Germany, in 1959. He received the Dipl.-Ing. and Ph.D. degrees in electrical engineering from the Technical University of Aachen, Germany, in 1985 and 1989, respectively. In 1983 he spent one year under a Fulbright Scholarship at the University of Cincinnati, OH.

He was with the CNET Research Center, Grenoble, France, from 1990 to 1991, working on silicon permeable base transistors. In 1991 he joined the Daimler-Benz AG Research Center, Ulm, Germany, where he is responsible for research and development of SiGe HBT's.

Friedrich Schäffler received the Diploma and Dr. rer. nat. degrees in physics from the Technical University Munich, Germany, in 1980 and 1984, respectively.

During 1985 and 1986 he was a post–doctoral research fellow at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY. In 1987 he became a member of the Scientific Staff the AEG Research Institute, Ulm, Germany, which became part of the Daimler-Benz Research Center in 1990. Mainly involved in the optical an electrical characterization of group IV and III–V structures and surfaces until 1987, he subsequently worked in the field of molecular beam epitaxy of Si and SiGe after joining AEG. There, his main activities have been the growth and characterization of high-performance two-dimensional electron and hole gases in modulation-doped Si/SiGe and SiGe/Ge heterostructures and the growth of homoepitaxial layer structures for mm-wave devices.

Dr. Schäffler is member of the American Vacuum Society and the American Physical Society.



Ulrich Guettich was born in Göttingen, Germany, in 1956. He received the Dipl.-Ing. and Dr.-Ing. degrees from the Technical University of Munich, Germany, in 1981 and 1986, respectively.

From 1981 to 1988 he worked at the Technical University of Munich in the field of BARITT and IMPATT device design and fabrication. In 1988 he joined the Millimeter Wave Department of Deutsche Aerospace A. G., Ulm, Germany, where he is currently involved in the development of planar integrated mm-wave circuits in microstrip and coplanar line techniques.

Andreas Klaaßen was born in Saarbrucken, Germany, on January 6, 1961. He received the Dipl.-Ing. degree in electrical engineering from the University of Saarland, Germany, in 1988.

Since 1988 he has been with the MIC/MMIC Design Center of the Deutsche Aerospace, Ulm, Germany. His current activities concern the development of millimeter-wave monolithic integrated circuits.